Atty. Docket No. PIA31224/DBE/US
Serial No: 10/751,198

Remarks

The Office Action dated May 20, 2005, which rejects claims 1-3, 7 and 11 under 35 U.S.C. 102(e) as being anticipated by Moon et al. (U.S. Pat. Appl. Publ. 2002/0164838), claims 4 and 8 under 35 U.S.C. 103(a) as being unpatentable over Moon et al. in view of Isaacson (U.S. Pat. No. 3,766,439), and claims 5, 6, 9 and 10 as being unpatentable over Moon et al. in view of Morrison et al. (U.S. Pat. Appl. Publ. 2002/0114143), has been carefully reviewed.

It is believed that Moon et al., Isaacson and Morrison et al. fail to disclose or suggest a method for packaging a multi-chip module, as recited in claim 1 above, wherein:

1. a first chip having thereon wafer bumps is connected to lower parts of inner leads of TAB tapes, each of the TAB tapes having an inner lead and an outer lead, thereby electrical signals being communicated therebetween;
2. a second chip having thereon wafer bumps is connected to an upper part of the TAB tapes connected to the first chip, thereby electrical signals being communicated therebetween;
3. an underfill material is filled in a connecting portion between the TAB tapes and the chips; and
4. the outer lead of one of the TAB tapes connected to the first chip is mounted on a patterned circuit.

Consequently, the presently claimed invention is believed to be fully patentable over Moon et al., Isaacson and Morrison et al., taken alone or together.

The Rejection of Claims 1-3, 7 and 11 under 35 U.S.C. § 102(e)

The rejection of Claims 1-3, 7 and 11 under 35 U.S.C. § 102(e) as being anticipated by Moon et al. is respectfully traversed.

Moon et al. discloses a method for increasing the integrated circuit density in a semiconductor assembly. The semiconductor assembly has an interposer substrate (which corresponds to the TAB tape of the present invention). The interposer substrate is attached to an active surface and a back side of a die. However, the interposer substrate in Moon et al. is connected to another assembly or a substrate using an array of conductive elements 172.

Accordingly, Moon et al. do not disclose the method of claim 1. It is further believed that the dies in Moon et al. are laminated more troublesomely than in the presently claimed invention. Therefore, it is respectfully submitted that claim 1 of the present invention define a patentable invention over Moon et al., and therefore, claim 1 is allowable.

Claims 2-3, 7 and 11, which directly or indirectly on amended claim 1, are also believed to be allowable for the same reasons indicated with respect to the claim 1, and further because of the additional features recited therein which, when taken alone and/or in combination with the features recited in claim 1, remove the invention defined therein further from the disclosure of the cited reference.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 4 and 8 under 35 U.S.C. § 103

The rejection of Claims 4 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Moon et al. in view of Isaacson is respectfully traversed.

Claim 4 depends from claim 1, and claim 8 depends from claim 2 (which, in turn, depends from claim 1. Therefore, claims 4 and 8 include the same limitations as claim 1 above. As explained above, the interposer substrate in Moon et al. is connected to another assembly or a substrate using an array of conductive elements 172, and the dies in Moon et al. are believed to be laminated more troublesomely than in the presently claimed invention. As will be explained below, it is believed that Isaacson fails to cure these deficiencies of Moon et al. Since Moon et al. does not have the inventive features of the present invention, the combination of Moon et al. and Isaacson does not disclose or suggest the presently claimed method. Thus, for essentially the

same reasons as for claim 1, claims 4 and 8 are believed to be patentable over Moon et al. in view of Isaacson.

Isaacson discloses an electronic circuit having utility in a multi-layer circuit board, formed of a flexible dielectric sheet of material to which is attached circuit runs etched from copper sheets clad to the dielectric sheet prior to etching (Abstract). It is believed that Isaacson fails to disclose or suggest a method for packaging a multi-chip module, as recited in claim 1 above, having at least one of the following attributes:

- a first chip having thereon wafer bumps is connected to lower parts of inner leads of TAB tapes, each of the TAB tapes having an inner lead and an outer lead, thereby electrical signals being communicated therebetween;
- a second chip having thereon wafer bumps is connected to an upper part of the TAB tapes connected to the first chip, thereby electrical signals being communicated therebetween;
- an underfill material is filled in a connecting portion between the TAB tapes and the chips; and
- the outer lead of one of the TAB tapes connected to the first chip is mounted on a patterned circuit.

Consequently, it is believed that Isaacson fails to cure all of these deficiencies of Moon et al. As a result, the presently claimed invention is believed to be fully patentable over Moon et al. and Isaacson, taken alone or together. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 5-6 and 9-10 under 35 U.S.C. § 103

The rejection of Claim 5-6 and 9-10 under 35 U.S.C. § 103 as being unpatentable over Moon et al. in view of Morrison et al. is respectfully traversed.

Claims 5-6 and 9-10 also depend from claim 1. Therefore, claims 5-6 and 9-10 include the same limitations as claim 1 above. As explained above, the interposer substrate in Moon et al. is connected to another assembly or a substrate using an array of conductive elements 172, and the dies in Moon et al. are believed to be laminated more troublesomely than in the presently claimed invention. As will be explained below, Morrison et al. fails to cure these deficiencies of Moon et al. Since Moon et al. does not have the inventive features of the present invention, the combination of Moon et al. and Morrison et al. does not disclose or suggest the presently claimed method. Thus, for essentially the same reasons as for claim 1, claims 5-6 and 9-10 are patentable over Moon et al. in view of Morrison et al.

Morrison et al. discloses a vertical stack of semiconductor devices, formed by folding a strip-like flexible interconnector assembled with integrated circuit chips, packages and/or passive components and attaching coupling members solderable to other parts (Abstract). It is believed that Morrison et al. fails to disclose or suggest a method for packaging a multi-chip module, as recited in claim 1 above, having at least one of the following attributes:

- a first chip having thereon wafer bumps is connected to lower parts of inner leads of TAB tapes, each of the TAB tapes having an inner lead and an outer lead, thereby electrical signals being communicated therebetween;
- a second chip having thereon wafer bumps is connected to an upper part of the TAB tapes connected to the first chip, thereby electrical signals being communicated therebetween;
- an underfill material is filled in a connecting portion between the TAB tapes and the chips; and
- the outer lead of one of the TAB tapes connected to the first chip is mounted on a patterned circuit.

Consequently, it is believed that Morrison et al. fails to cure all of these deficiencies of Moon et al. As a result, the presently claimed invention is believed to be fully patentable over

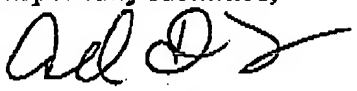
Moon et al. and Morrison et al., taken alone or together. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

## Conclusions

In view of the above amendments and remarks, all grounds for rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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